**Q3**

**a) Main Features of a Field Effect Transistor (FET)**

* Unipolar Device: FETs use either electrons (n-channel) or holes (p-channel) as charge carriers, making them unipolar devices, unlike bipolar junction transistors (BJTs) that use both types of charge carriers.
* High Input Impedance: FETs have very high input impedance, typically in the range of megaohms (MΩ) to gigaohms (GΩ), which results in minimal loading of the preceding stage.
* Voltage-Controlled Device: The current through the FET is controlled by the voltage applied to the gate terminal, rather than the current, making it a voltage-controlled device.
* Low Power Consumption: Due to their high input impedance and low current drive requirements, FETs typically consume less power than BJTs.
* Thermal Stability: FETs are generally more thermally stable than BJTs, with less variation in performance over temperature changes.
* Types of FETs: There are several types of FETs, including Junction FETs (JFETs) and Metal-Oxide-Semiconductor FETs (MOSFETs).

**b) Main Advantages of a MOSFET**

* High Input Impedance: MOSFETs have even higher input impedance than JFETs, often exceeding several gigaohms (GΩ).
* Fast Switching Speed: Due to the small gate charge and capacitance, MOSFETs can switch on and off rapidly, making them ideal for high-speed and high-frequency applications.
* Low On-Resistance: When turned on, MOSFETs can have very low resistance between the drain and source, resulting in efficient conduction and low power dissipation.
* Scalability: MOSFETs can be easily scaled down in size, making them suitable for integrated circuits and very-large-scale integration (VLSI).
* Low Power Consumption: In digital circuits, MOSFETs consume very little power when switching states, as the gate current is negligible.
* Complementary MOS (CMOS) Technology: MOSFETs are fundamental components in CMOS technology, which is the backbone of modern digital electronics, allowing for low power consumption and high-density integration.

**c) IV Graph for a MOSFET in Depletion Mode**

**Drawing the IV Graph:**

1. **Axes**:
   * The horizontal axis (x-axis) represents the Drain-Source Voltage (VDS).
   * The vertical axis (y-axis) represents the Drain-Source Current (IDS) .
2. **Regions**:
   * **Ohmic Region**: At low (VDS)​, the MOSFET operates in the linear or ohmic region, where (IDS)increases linearly with VDS.
   * **Saturation Region**: At higher VDS​, the MOSFET enters saturation, where IDS becomes relatively constant and independent of VDS​.
3. **Depletion Mode Operation**:
   * In depletion mode, the MOSFET can conduct current even when the gate-source voltage (VGS)is zero or negative.
   * The graph shows the relationship between IDS​ and VDS​ for different values of VGS.

**Indicating IDS= 1.2 mA on the Graph:**

* Draw a horizontal line at **IDS= 1.2 mA**.
* This line intersects the IDS-VDS​ curves for various VGS values.
* Highlight the intersection point on the graph to indicate **IDS= 1.2 mA.**

Here's a simplified sketch of the IV characteristics for a depletion-mode MOSFET:

I\_{DS} (mA)

|

| \ \ \

1.2|---- \---\---\--------------- (indicating the current value)

| \ \ \

| \ \ \

| \ \ \

|\_\_\_\_\_\_\_\_\_\\_\_\_\\_\_\_\\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ V\_{DS}

In a real graph:

* The curves for different VGS​ values will be shown.
* IDS ​=1.2 mA will be marked on the appropriate curve(s) based on the given VGS.

**Q4**

**Design**

* First we make 3 bit-asynchronous counter using j-k flip flop by help of 4- bit -asynchronous counter.
* Then by using three outputs Q0,Q1,Q2 of counter as input impulse to get A,B,C,D outputs.
* K-maps to make logic A, B, C, D are:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| A =Q0\Q1.Q2 | 00 | 01 | 11 | 10 |
| 0 | 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 | 1 |

A=Q0.Q1’+Q1’.Q2+Q1.Q2’

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| B =Q0\Q1.Q2 | 00 | 01 | 11 | 10 |
| 0 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 1 | 1 |

B=Q2+Q0.Q2

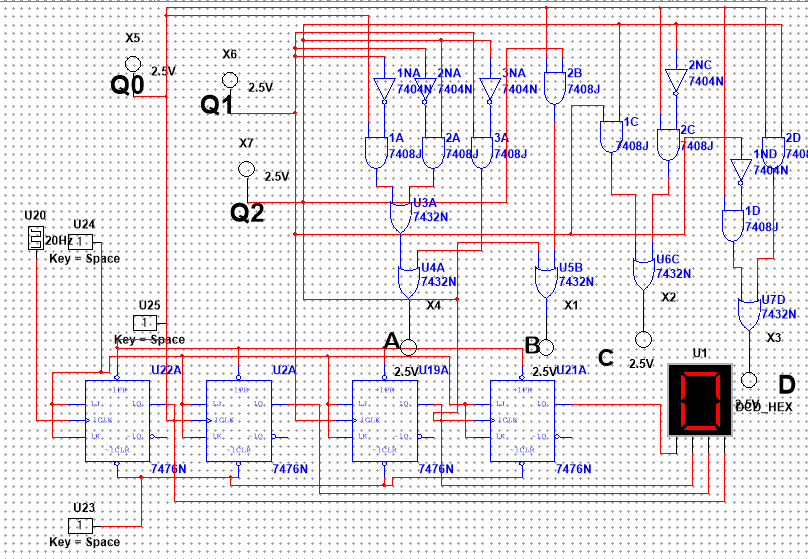
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| C =Q0\Q1.Q2 | 00 | 01 | 11 | 10 |
| 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 | 1 |

C=Q1.Q2+Q0.Q2’

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| D =Q0\Q1.Q2 | 00 | 01 | 11 | 10 |
| 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 |

D=Q0.Q1’+Q0.Q2

CIRCUIT IMAGE



TRUTH TABLE:

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| input | Q2 | Q1 | Q0 | D | C | B | A |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 2 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| 3 | 0 | 1 | 1 | 0 | 1 | 1 | 0 |
| 4 | 1 | 0 | 0 | 1 | 1 | 0 | 1 |
| 5 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| 6 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |
| 7 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 9 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |